Voltage Skew-Based Test Technique for Pre-Bond TSVs in 3-D ICs

Jun Liu, Zhi Chen, Tian Chen, Xi Wu, Huaguo Liang, and Xiaohui Yuan, *Senior Member, IEEE*

***Abstract*—In 3D ICs, the manufacturing process of through silicon via (TSV) is still immature, which can result in resistive open faults and leakage faults. Pre-bond TSV tests can effectively improve the performance and yield of 3D ICs. In this brief, a new pre-bond TSV test method based on the voltage skew is proposed. The proposed method charges a pre-set load capacitor during the voltage skew between faulty and fault-free TSV. It then measures the charge time to detect TSV faults. Furthermore, a variable drive inverter is designed to change the duration of voltage skew and recharge the load capacitor. By comparing the twice charge time, the type of TSV faults can be identified. The experimental results show that the proposed method can detect resistive open faults with $R_{open} \geq 400\Omega$ and leakage faults with $R_{leak} \leq 20M\Omega$. Compared to other test methods, the proposed method has higher detection capability.**

***Index Terms*—3-D ICs, through silicon via (TSV), resistive open fault, leakage fault, pre-bond TSV test, voltage skew.**

I. Introduction

COMPARED to traditional two-dimensional integrated circuits, three-dimensional integrated circuits(3D ICs) have tremendous advantages, such as higher bandwidth, lower power, and greater integration capabilities [1], [2]. However, the TSV manufacturing process is not yet mature, which may result in resistive open faults and leakage faults [3], [4]. TSV faults can directly affect the yield and performance of 3D ICs [5], [6]. To ensure the yield of 3D ICs, the TSV test is essential. TSV test is categorized into pre-bond test and post-bond test [7]. The pre-bond test detects TSV faults during the manufacturing process, while the post-bond test detects faults during the stacking process. Failing to detect a TSV fault before bonding may result in the failure of the entire chip after bonding, leading to a significant increase in manufacturing costs [8]. Therefore, pre-bond test must be investigated.

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Cho et al. [9] and Lin et al. [10] proposed the methods for fault detection by measuring the top voltage of TSV. However, these methods are not capable of detecting the resistive open faults in TSV as they do not affect the top voltage. As a result, these methods are only applicable to the detection of TSV leakage faults. The ring oscillator-based solutions [11], [12] are effective in detecting resistive open faults and leakage faults. In these methods, the TSV is modeled as an RC delay circuit and incorporated into the ring oscillator. As both resistive open faults and leakage faults change the delay of the ring oscillator, the faults can be detected by measuring the oscillation period. However, weak faults have a minimal impact on the oscillation period, making it difficult to measure the slight difference in the oscillation period between faulty and fault-free TSVs. Thus, the test accuracy of methods [11], [12] is limited.

Besides the ring oscillator methods, the methods based on TSV charge or discharge can also detect resistive open faults and leakage faults. Di Natale et al. [13] and Xu et al. [14] proposed the methods for measuring the TSV discharge time. Because both resistive open faults and leakage faults reduce the discharge time, the methods can detect the occurrence of faults, but they are unable to identify the specific type of faults. To identify the type of faults, Das et al. [15] proposed a method based on the TSV charge time. Because the resistive open fault reduces charge time while the leakage fault increases the charge time, this method can identify the fault type based on the charge time of TSV. However, when the TSV fault is weak, the charge(discharge) time difference between faulty and fault-free TSVs is also minor and difficult to measure. Therefore, the test accuracy of these methods is also not high.

To improve the test accuracy and identify different types of TSV faults, this brief proposes a Voltage Skew-based Test (VST) solution for pre-bond TSV. The voltage skew refers to the phase deviation between output signals of faulty and fault-free TSV. The VST method firstly charges a pre-set load capacitor during voltage skew. If the charge time differs from that of a fault-free TSV, it indicates the corresponding TSV is faulty. Subsequently, custom-designed variable drive inverters are utilized to alter the duration of voltage skew to recharge the load capacitor. Through the comparison of the twice charge time, the VST method can identify resistive open faults and leakage faults. It should be noted that the VST method doesn't directly measure the charge time of TSV. Rather, it measures the charge time of the pre-set load capacitor. This can increase the difference in charge time between faulty and fault-free TSVs, thereby effectively enhancing the test accuracy.

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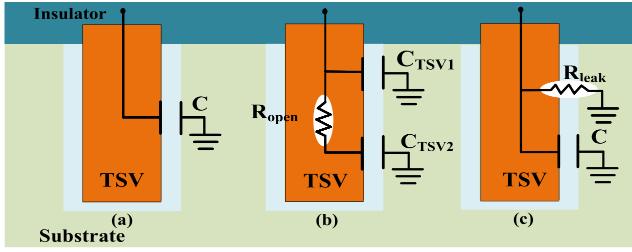


Fig. 1. TSV electrical models:(a) fault-free. (b) resistive open fault. (c) leakage fault.

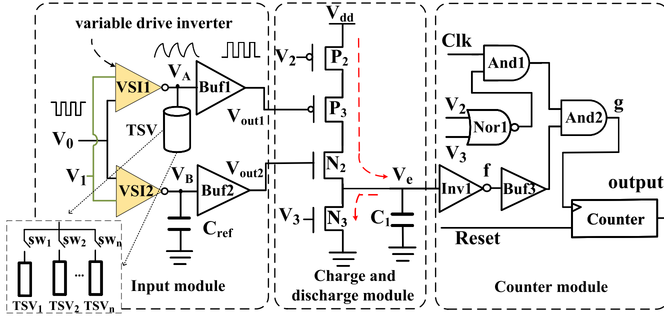


Fig. 2. The test structure of the VST method.

II. TSV Electrical Model

Fig. 1(a) is the electrical model of a fault-free TSV during the pre-bond stage. In this model, the TSV is represented by a capacitor denoted as C [16], [17].

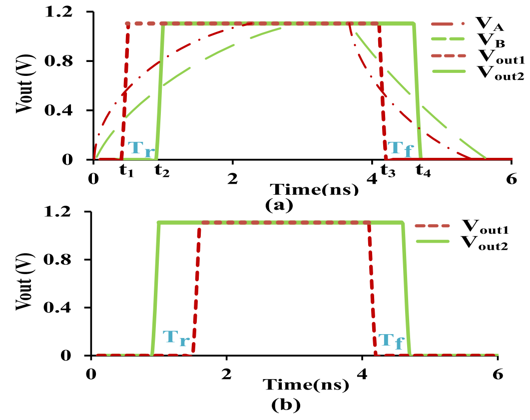
The resistive open fault is illustrated in Fig. 1(b). This fault results from a micro-void defect within the TSV and can be represented as a resistor R_{open} [18]. The R_{open} divides the TSV equivalent capacitance into two parts, the upper portion with a capacitance of $C_{TSV1} = x * C$ and the lower portion with $C_{TSV2} = (1 - x) * C$, where $x(0 < x < 1)$ represents the distance from the void to the top of the TSV. The more severe the micro-void defect, the greater the value of R_{open}.

Fig. 1(c) depicts the leakage fault, which occurs when pinholes are present in the silicon dioxide [19]. The pinhole creates a leakage path from the TSV to the substrate and is modeled as a resistance R_{leak}. As the severity of the leakage fault increases, the value of R_{leak} decreases.

III. The VST Method

A. Test Structure

The test structure of the proposed VST method is depicted in Fig. 2. This structure comprises three modules: an input module, a charge and discharge module, and a counter module. The input module generates the voltage skew. The charge and discharge module is responsible for charging and discharging the load capacitor C_1. The counter module measures the charge time of C_1. To mitigate hardware overhead, the VST method utilizes multiple TSVs to share the test circuit. In this structure, the test circuit employs a transmission gate SW to select a TSV for testing. only one transmission gate is active during each test, while the others are deactivated.



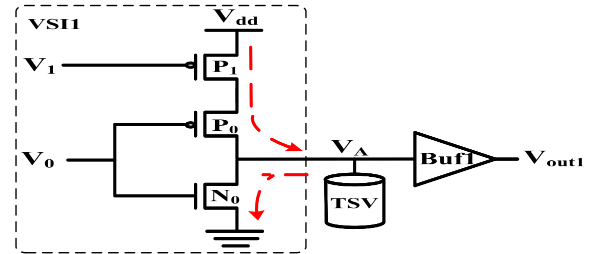


Fig. 3. Voltage skew under different types of TSV faults. (a) resistive open fault. (b) leakage fault.

Fig. 4. Circuit structure of VSI1.

1) Input Module: The input module consists of custom-designed variable drive inverters(VSI1 and VSI2), buffers (Buf1 and Buf2), and one capacitor(C_{ref}). The capacitance value of C_{ref} corresponds to the equivalent capacitance of fault-free TSV. The voltage at the top of the TSV is denoted as V_A, and the voltage at the C_{ref} node is denoted as V_B. V_{out1} and V_{out2} are the output signals of Buf1 and Buf2, respectively.

When the TSV is fault-free, the V_A and V_B have the same value. Consequently, V_{out1} and V_{out2} completely overlap without voltage skew.

When the TSV experiences a resistive open fault, its equivalent capacitance reduces, leading to a decrease in the charge and discharge time. Therefore, during the charging of the faulty TSV, V_A reaches the threshold voltage of BUF before V_B. As shown in Figure 3(a), V_A and V_B reach the threshold voltage of BUF at time t_1 and t_2, respectively, resulting in an earlier transition of V_{out1} compared to V_{out2}. This causes a voltage skew for the positive transition, with a duration of $T_r = t_2 – t_1$. Similarly, when the faulty TSV discharges, V_A also drops to the threshold of BUF before V_B, causing the negative transition of V_{out1} to occur earlier than that of V_{out2}. This results in a voltage skew for the negative transition, with a duration of $T_f = t_4 – t_3$. In case of leakage faults in the TSV, its charge time increases, while the discharge time decreases. V_{out1} and V_{out2} also exhibit positive and negative transition voltage skew, as Figure 3(b) shows.

The VSI1 and VSI2 in Fig. 2 are the variable drive inverters. The circuit structure of VSI1 is shown in Fig. 4. Different from conventional inverters, this structure requires an additional transistor P_1. The VSI1 and VSI2 can change the duration of voltage skew between V_{out1} and V_{out2} by adjusting the value of V_1.

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TABLE I
THE TRANSITION MOMENT FOR RESISTIVE OPEN FAULT ($R_{open} = 20K\Omega$)

V_1	Positive transition		T_r	Negative transition		T_f
	V_{out1}	V_{out2}		V_{out1}	V_{out2}	
0.2V	1.35ns	1.63ns	0.28ns	7.54ns	7.73ns	0.19ns
0 V	1.12ns	1.38ns	0.26ns	7.54ns	7.73ns	0.19ns

TABLE II
THE TRANSITION MOMENT FOR LEAKAGE FAULT ($R_{leak} = 100K\Omega$)

V_1	Positive transition		T_r	Negative transition		T_f
	V_{out1}	V_{out2}		V_{out1}	V_{out2}	
0.2V	1.73ns	1.63ns	0.10ns	7.65ns	7.73ns	0.08ns
0 V	1.44ns	1.38ns	0.06ns	7.65ns	7.73ns	0.08ns

Table I shows the transition moments of V_{out1} and V_{out2}, along with the duration of voltage skew when the TSV has a resistive open fault. For V_1 equal to 0.2V, the positive transition of V_{out1} and V_{out2} occurs at 1.35ns and 1.63ns, respectively, and T_r is 0.28ns (1.63–1.35). The negative transition of V_{out1} and V_{out2} happens at 7.54ns and 7.73ns, respectively, and T_f is 0.19ns.

Table II depicts the transition moments and voltage skew when the TSV has a leakage fault. As shown in Table II, when V_1 decreases from 0.2V to 0V, T_r reduces from 0.10ns to 0.06ns, while T_f remains at 0.08ns.

From Table I and Table II, it can be inferred that when TSV has resistive open or leakage fault, a decrease in V_1 leads to a reduction in T_r, while T_f remains unchanged. The proof procedure is as follows:

The time t_A and t_B for V_A and V_B rise to the threshold voltage (V_{th}) of Buf1 and Buf2 are:

$$t_A = RC_{fault} \ln\left(\frac{V_{dd}}{V_{dd} - V_{th}}\right) \quad (1)$$

$$t_B = RC_{ref} \ln\left(\frac{V_{dd}}{V_{dd} - V_{th}}\right) \quad (2)$$

where R represents the total resistance of transistors P_0 and P_1 in Fig. 4. C_{fault} and C_{ref} are the equivalent capacitance of faulty and fault-free TSV, respectively.

From Eq. (1) and Eq. (2), we can calculate T_r:

$$T_r = |t_B - t_A| = \left|R\left(C_{ref} - C_{fault}\right) \ln\left(\frac{V_{dd}}{V_{dd} - V_{th}}\right)\right| \quad (3)$$

When V_1 decreases, the total resistance R decreases, while other parameters in Eq. (3) remain unchanged. Therefore, as V_1 decreases, the T_r reduces.

The following clarifies the reason why T_f remains unchanged. In Fig. 4, when the voltage V_0 is high, the transistor P_0 is turned off and the transistor N_0 is turned on, allowing the TSV to discharge through N_0. As the P_0 is turned off, the gate voltage V_1 of transistor P_1 has minimal effect on the discharge current of the TSV. Consequently, the negative transition moment of both V_{out1} and V_{out2} does not change, resulting in an unchanged T_f.

2) Charge and Discharge Module: The middle part of the Fig. 2 is the charge and discharge module. When voltage V_2 and V_3 are low, P_2 is turned on while N_3 is turned off, indicating that the module is in charge mode.

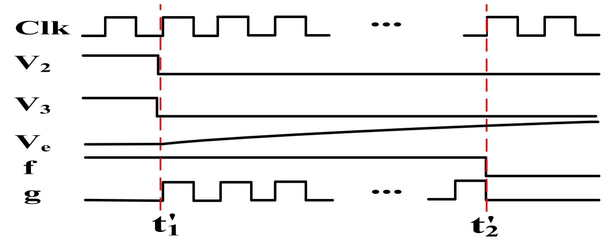

Fig. 5. Timing diagram of the charge process.

If a resistive open fault occurs in the TSV, capacitor C_1 will only be charged during T_f shown in Fig. 3(a). During T_f, both P_3 and N_2 are turned on, allowing V_{dd} to charge C_1. Outside of T_f, P_3 and N_2 cannot be turned on simultaneously, and as a result, C_1 cannot be charged.

If there is a leakage fault in the TSV, capacitor C_1 will be charged during the T_r and T_f as shown in Fig. 3(b). This is because both P_3 and N_2 can be turned on during the T_r and T_f, enabling the charge of C_1.

In the case of fault-free TSV, V_{out1} and V_{out2} completely overlap. The capacitor C_1 can only be charged during the transition phase of V_{out1} and V_{out2}, which is significantly shorter than the duration of T_r and T_f. Consequently, it takes a much longer time to fully charge the capacitor C_1 compared to a faulty TSV.

When both V_2 and V_3 are high, transistor P_2 is turned off while transistor N_3 is turned on. This causes the charge and discharge module to operate in discharge mode. In this mode, capacitor C_1 can discharge through N_3 to the ground.

3) Counter Module: The function of the counter module is to measure the charge time of the load capacitance C_1. The timing diagram of the charge process is depicted in Fig. 5.

When both V_2 and V_3 are low, the charge and discharge module initiates the charge of capacitor C_1, and the counter module commences counting. Once the voltage V_e at C_1 node surpasses the threshold voltage of inverter Inv1 in Fig. 2, the counter will cease its counting process. In Fig. 5, at the time t_1' and t_2', the counter starts and stops counting, respectively. The value of the counter represents the charge time of C_1.

B. Test Flow of VST Method

Figure 6 illustrates the TSV test flow of the proposed VST method, consisting of two stages: the first charge stage and the second charge stage. During the first charge stage, if the charge time of capacitor C_1 is shorter than the reference time, it indicates a fault in the TSV. The reference time corresponds to the charge time of C_1 when the TSV is fault-free. Although the first charge stage can detect faults, it cannot identify the specific type of TSV faults. To identify these faults, we decrease V_1 in Fig. 4 to change the duration of voltage skew and recharge C_1 after it has been completely discharged.

When TSV has a resistive open fault, only during T_f, will capacitor C_1 be charged. At any other time, C_1 will not be charged. Therefore, the second charge time should be equal to the first charge time since the T_f remains unchanged when the voltage V_1 decreases.

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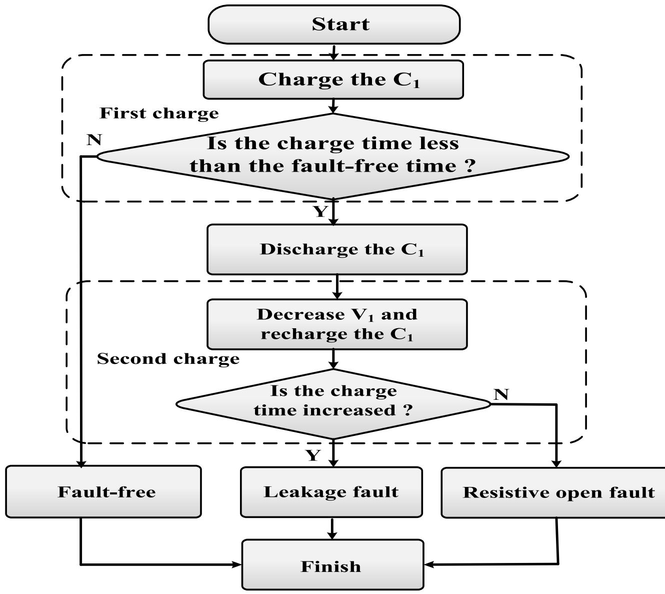

Fig. 6. The test flow of VST method.

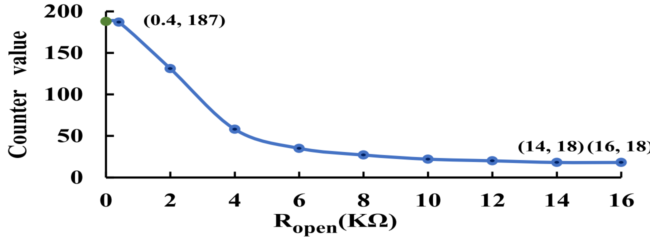

Fig. 7. The counter value of different R_{open}.

In the case of leakage faults, the C_1 will be charged during both the T_r and T_f. Consequently, the second charge time will be longer than the first charge time due to the reduced T_r and unchanged T_f. In conclusion, the type of TSV faults can be identified based on the twice charge time.

IV. Experimental Results and Analysis

To evaluate the effectiveness of the VST method, the HSPICE tool is used to simulate the test circuit with 45nm PTM (Predictive Technology Model) CMOS process [20], [21]. According to the [12], C_{ref} is set to 60fF. To balance the test accuracy and the hardware overhead, the C_1 and CLK are set to 35fF and 2ns, respectively.

A. Detecting the TSV Faults

Figure 7 illustrates the correlation between resistance open faults and the charge time of capacitor C_1. The X-axis is the value of R_{open}, while the Y-axis represents the counter value. During the charge period of the load capacitor C_1, the counter value increases by 1 for each clock cycle. Therefore, the counter value multiplied by the clock cycle of 2ns gives the charge time of C_1. For convenience, the counter value is used to represent the charge time of capacitors. Figure 7 shows that as the R_{open} increases from 0 to 16KΩ, the counter value decreases from 188 to 18. When R_{open} is 0, the TSV is fault-free, and the corresponding counter value is 188. Once R_{open} exceeds 0.4KΩ, the counter value starts to change, indicating the faults can be detected.

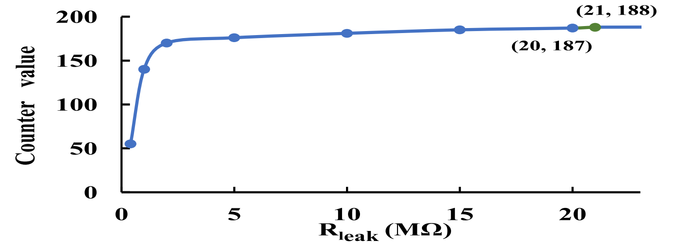

Fig. 8. The counter value of different leakage faults.

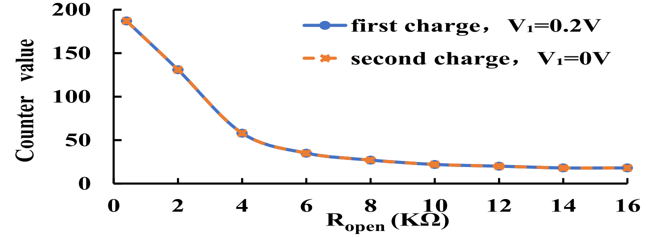

Fig. 9. The twice charge time for different resistive open faults.

Figure 8 depicts the correlation between TSV leakage faults and the charge time of C_1. The X-axis represents the leakage fault resistance R_{leak}, where smaller values indicate more severe leakage faults. From Figure 8, we can observe that the charge time increases with the increase of R_{leak}. This is because as R_{leak} increases, the leakage fault weakens, resulting in a smaller voltage skew and a charge time closer to the reference time. Furthermore, Figure 8 shows that when R_{leak} exceeds 20MΩ, the counter value stabilizes at 188. This implies that the leakage fault is too weak to be detected. Therefore, the VST method can detect the leakage faults when the R_{leak} is less than or equal to 20MΩ.

Process variation can result in the decrease of test accuracy. We conduct 1000 simulations, wherein process variation varies within ±5% of their nominal values, following a Gaussian distribution. As a result, we obtain the charge time of the load capacitor C_1 when the TSV is fault-free, with a maximum value of 191 and a minimum value of 182. Therefore, as long as the charge time of C_1 falls within the range of [182, 191], the TSV is considered fault-free. Under the process variation, the proposed VST method is capable of detecting resistive open faults with $R_{open} \geq 0.8$KΩ and leakage faults with $R_{leak} \leq 16$MΩ.

B. Identifying the Type of Faults

Figure 9 shows the twice charge time of C_1 when TSV has a resistive open fault. We can see that the twice charge time is equal. For instance, when the R_{open} is 0.4KΩ, both the first and second charge time is 187.

Table III presents the twice charge time of C_1 when TSV has a leakage fault. The twice charge time is different. For example, when the R_{leak} is 400KΩ, the first charge time is 55, while the second is 75. Table III indicates that as R_{leak} increases, the difference between the first and the second charge time gradually decreases. This is because a higher R_{leak} corresponds to a weaker leakage fault and a smaller

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TABLE III
THE TWICE CHARGE TIME FOR DIFFERENT LEAKAGE FAULTS

$R_{leak}(\Omega)$	400K	1M	5M	20M
First charge time	55	140	180	187
Second charge time	75	152	184	188

TABLE IV
COMPARISON RESULTS WITH OTHER METHODS

Methods	$R_{open}(\Omega)$	$R_{leak}(\Omega)$	Identify faults	overhead (um^2)
[9]	undetected	1M	×	92.7
[10]	undetected	5M	×	5.32
[11]	5k	50k	√	49.0
[13]	6K	10M	×	15.8
[14]	30K	200M	×	73.8
[15]	3K	10M	√	51.9
VST	0.4K	20M	√	55.4

voltage skew. Consequently, the charge time of capacitor C_1 increases and approaches the reference time as R_{leak} increases. Additionally, the influence of voltage V_1 on the charge time diminishes as R_{leak} increases.

C. Comparison With Other Methods

Finally, we compared the VST method with other pre-bond TSV test techniques. To ensure fairness, we simulated all the techniques using the 45nm PTM CMOS process in HSPICE simulations. The comparison results are shown in Table IV.

Table IV demonstrates that the VST method is capable of detecting resistive open faults with $R_{open} \geq 0.4\text{K}\Omega$, which surpasses all other techniques. In terms of leakage faults, the VST method can detect leakage faults with $R_{leak} \leq 20\text{M}\Omega$, which outperforms most methods except for [14]. Furthermore, the proposed method can identify resistive open faults and leakage faults, whereas some methods [9], [10], [13] and [14] do not have this capability. The hardware overhead of the VST method is $55.4um^2$, which is larger than [10], [11], [13], and [15]. This is mainly due to the counter, which occupies a significant hardware cost. Since multiple TSVs can share the test circuit of the VST method, if the hardware overhead is distributed among them, the overhead for testing a single TSV will be significantly reduced.

V. CONCLUSION

In this brief, we propose a pre-bond TSV test method called VST method. The VST method utilizes the voltage skew between faulty and fault-free TSVs to charge a pre-set load capacitor twice. Based on the charge time, the VST method can determine whether the TSV is faulty. For the faulty TSV, the method uses the custom-designed variable drive inverter to change the duration of voltage skew and recharge the load capacitor. By comparing the twice charge time, the VST method can identify resistive open faults and leakage faults. Experimental results show that the proposed technique can detect resistive open faults with $R_{open} \geq 0.4\text{K}\Omega$ and leakage faults with $R_{leak} \leq 20\text{M}\Omega$.

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